LISTING OF THE CLAIMS

Please amend claims 1-7, and enter new clams 8-14 as indicated below. This listing of claims replaces al prior versions.

1. (Currently Amended) A dual residue pipelined AD-converter for converting an analog input signal to a digital output signal, said converter comprising

a cascade of dual residue converter stages,

~~the first of said stages comprising means to receive the analog input signal, means to derive one or more digital bits from said analog input signal and means to generate first and second residue signals representing the quantization error left after the AD-conversion of said first stage,~~

~~each of the following~~ at least two stages in the cascade of dual residue converter stages ~~comprising~~ each including

switched capacitor means to receive ~~the first and second~~ two residue signals generated by ~~the~~ a previous stage in the cascade, one of the residue signals representing quantization error relative to a first quantization level and the other one of the residue signals representing quantization error relative to a second quantization level,

means to derive one or more ~~further~~ digital bits from said received ~~first and second~~ residue signals, and ~~each of said following stages except the last one in the cascade comprising~~

means to generate a respective first residue signal representing quantization error relative to a first quantization level and a respective second residue signal representing quantization error relative to a second quantization level, the first and second residue signals representing the quantization error resulting from ~~left after the~~ an AD-conversion ~~of the stage, characterized in that each of the stages of the dual residue pipelined AD-converter, except the last one, comprises switched capacitor means for the generation of the first and second residue signals~~.

2. (Currently Amended) A dual residue pipelined AD-converter as claimed in claim 1 characterized in that ~~each of said following~~ the at least two stages each ~~except the last one comprise~~ include input capacitors for receiving during a sampling phase the ~~first and second~~ two residue signals generated by the previous stage, switching means ~~(φ)~~ to transfer during a tracking phase the charge of said input capacitors to first and second output capacitors, and means to generate the respective first and second residue signals from said first and second output capacitors respectively.

3. (Currently Amended) A dual residue pipelined AD-converter as claimed in claim 2 characterized in that said switching means ~~(φ)~~ are arranged to transfer charge from ~~said first~~ one of the received residue signals to said first output capacitor with a gain factor of approximately 2 and charge from both said ~~first and second~~ received residue signals to said second output capacitor each with a gain factor of approximately 1 in a first sub-range mode ~~($D_2 = 0$)~~ and to transfer charge from ~~said second~~ the other one of the received residue signals to said second output capacitor with a gain factor of approximately 2 and charge from both said ~~first and second~~ received residue signals to said first output capacitor each with a gain factor of approximately 1 in a second sub-range mode ~~($D_2 = 1$)~~.

4. (Currently Amended) A dual residue pipelined AD-converter as claimed in claim 3 characterized in that said switching means are additionally arranged to transfer charge from both said ~~first and second~~ received residue signals to said first output capacitor with a gain factor of approximately 3/2 and 1/2 respectively and charge from both said ~~first and second~~ received residue signals to said second output capacitor with a gain factor of approximately 1/2 and 3/2 respectively in a third sub- range mode ~~($E = 1$)~~ which lies symmetrically between said first and second sub-range modes.

5. (Currently Amended) A dual residue pipelined AD-converter as claimed in claim 2 characterized in that for the generation of each residue signal an operational amplifier is provided and that each output capacitor is connected during the tracking phase ~~(φ)~~ between an output terminal and the inverting input terminal of said operational amplifier.

6. (Currently Amended) A dual residue pipelined AD-converter as claimed in claim 5 characterized in that one side of each input capacitor is connected to said inverting input terminal both during the sampling phase ~~(φ)~~ and during the tracking phase ~~(φ)~~ and that each output capacitor is charged during the sampling phase by the offset voltage at the inverting input of the operational amplifier.

7. (Currently Amended) A dual residue pipelined AD-converter as claimed in claim 1, characterized in that the two residue signals are ~~in that the switched capacitor means~~ are ~~arranged to receive~~ balanced signals and the respective first and second residue signals ~~and to generate there from~~ are balanced ~~first and second residue~~ signals ~~for application to the next stage in the cascade~~.

8. (New) A dual residue pipelined AD-converter for converting an analog input signal to a digital output signal, said converter comprising a cascade of dual residue converter stages,

the first of said stages including means to receive the analog input signal, means to derive one or more digital bits from said analog input signal and means to generate first and second residue signals representing the quantization error left after the AD-conversion of said first stage, and

each of the following stages in the cascade of dual residue converter stages including means to receive respective first and second residue signals generated by the previous stage in the cascade, means to derive one or more further digital bits from said received first and second residue signals and each of said following stages except the last one in the cascade include input capacitors for receiving during a sampling phase the first and second residue signals generated by the previous stage, switching means to transfer during a tracking phase the charge of said input capacitors to first and second output capacitors, and means to generate first and second residue signals representing the quantization error left after the AD-conversion of the stage from said first and second output capacitors respectively,

characterized in that said switching means are arranged to transfer charge from said first received residue signal to said first output capacitor with a gain factor of approximately 2 and charge from both said first and second received residue signals to said second output capacitor each with a gain factor of approximately 1 in a first sub-range mode and to transfer charge from said second received residue signal to said second output capacitor with a gain factor of approximately 2 and charge from both said first and second received residue signals to said first output capacitor each with a gain factor of approximately 1 in a second sub-range mode.

9. (New) A dual residue pipelined AD-converter as claimed in claim 8 characterized in that for the generation of each residue signal an operational amplifier is provided and that each output capacitor is connected during the tracking phase between an output terminal and the inverting input terminal of said operational amplifier.

10. (New) A dual residue pipelined AD-converter as claimed in claim 9 characterized in that one side of each input capacitor is connected to said inverting input terminal both during the sampling phase and during the tracking phase and that each output capacitor is charged during the sampling phase by the offset voltage at the inverting input of the operational amplifier.

11. (New) A dual residue pipelined AD-converter as claimed in claim 8, characterized in that each of said following stages except the last one in the cascade are arranged to receive balanced first and second residue signals from the previous stage and to generate therefrom balanced first and second residue signals for application to the next stage in the cascade.

12. (New) A dual residue pipelined AD-converter for converting an analog input signal to a digital output signal, said converter comprising a cascade of dual residue converter stages,

the first of said stages including means to receive the analog input signal, means to derive one or more digital bits from said analog input signal and means to generate

first and second residue signals representing the quantization error left after the AD-conversion of said first stage, and

each of the following stages in the cascade of dual residue converter stages including means to receive the first and second residue signals generated by the previous stage in the cascade, means to derive one or more further digital bits from said received first and second residue signals and each of said following stages except the last one in the cascade include input capacitors for receiving during a sampling phase the first and second residue signals generated by the previous stage, switching means to transfer during a tracking phase the charge of said input capacitors to first and second output capacitors, and means to generate first and second residue signals representing the quantization error left after the AD-conversion of the stage from said first and second output capacitors respectively,

characterized in that for the generation of each residue signal an operational amplifier is provided and that one side of each input capacitor is connected to the inverting input terminal of the operational amplifier both during the sampling phase and during the tracking phase and that each output capacitor is charged during the sampling phase by the offset voltage at the inverting input of the operational amplifier.

13. (New) A dual residue pipelined AD-converter as claimed in claim 12 characterized in that each output capacitor is connected during the tracking phase between an output terminal and the inverting input terminal of said operational amplifier.

14. (New) A dual residue pipelined AD-converter as claimed in claim 12, characterized in that each of said following stages except the last one in the cascade are arranged to receive balanced first and second residue signals from the previous stage and to generate therefrom balanced first and second residue signals for application to the next stage in the cascade.